**Pavan Kumar Gopalapuram**

M.Tech in VLSI & ES, Mobile: +91-9290659978

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| **Objective** |

Seeking a position with an organization where I can contribute my skills for organization’s success and synchronize with new technology while being resourceful, innovative and flexible.

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| **Skill Set** |

* + EDA Tools : Mentor FPGA Advantage, Multisim, LT Spice, KEIL

 ALTERA Quartus – II, PSoC Designer, PSoC Express,

 Tanner Tools, H-spice.

* + Hardware Description Languages : Verilog, system verilog.
	+ Software Skills : C, Shell Scripting, Perl, HTML, PHP.
	+ Platforms : UNIX, Windows.
	+ Architectures : µP 8085, µC 8051.
	+ Assembly Programming : µP 8085, µC 8051.
	+ Hardware Expertise : Cypress PSoC Board (for Embedded Applications),

 Altera FPGA Board (Processor Based System Design)

* + Mathematical Tools : MATLAB.

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| **Technical Expertise** |

Analog & Mixed Signal Circuit Design, Digital Design, Adaptive Signal processing, Microprocessors, Microcontrollers & Interfacing, Embedded Systems, Computer Organization & Architecture, Programmable SoC (for Embedded Applications), FPGA Based System Design, Low Power CMOS VLSI Design, Microelectronics, VLSI Digital Signal Processing Systems, ASIC & FPGA Flow.

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| **Academic Profile** |

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| **Degree** | **Board / University** | **Year**  | **CGPA / Percentage** |
| M.Tech [VLSI & Embedded Systems] | IIIT-Hyderabad | 2006 - 2008 |  **7.03/10** |
| B.E [ECE] | Osmania University | 2001 - 2005 | **72.05%** |

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| **Achievements** |

* Secured Score of 463 with 1327th rank among 36,500 aspirants in GATE’ 06.
* Presented a Paper on ’speech coding’ at National level technical meet Organized by Dept. of E.C.E. Deccan College of Engineering and Technology.
* I was the leader in managing team for the national level technical feast conducted by our department in the college.
* Won First prize twice and second prize once in Essay writing competition at Junior college Level and city level.

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| **Current status** |

* Currently working as Research assistant in CVEST (Centre for VLSI and Embedded system Technology under Dr. Mandavilli Satyam in IIIT Hyderabad.

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| **Projects** |

**M.Tech Final Year Project**

1. Title: **Designing of Analog PLL and Layout designing**.

Abstract: I have successfully Designed all the blocks of a PLL along with an Automatic gain control circuit in 1 μm CMOS Technology and integrated them for testing the PLL circuit. The fundamental frequency of the PLL is 30MHz and the VCO can vary between 28.5MHz and 31MHz frequencies for ±1v variation in the control voltage. The PLL mentioned is made immune to the variations of the input signal amplitude between 500mv to 1100mv with the help of an Automatic gain control system. The total number of MOSFETs in this Design are 106. Layout design is carried out for VCO and Phase detector. Entire Project is done in Tanner tools version 7.10. This project is done as a part of Research assistantship at CVEST in IIIT Hyderabad. **Team Size: 1**

**M.Tech Semester projects**

1. Title: **Development of a Virtual Machine for TMS320C54X and Implementing up sampling algorithm.**

 Abstract: The virtual machine is developed using Microsoft Visual C++. A Human Machine Interface is created, which helps the user to design a code for TMS320C54X to implement on the virtual machine. **Team Size: 5**

1. Title: **Design of Translinear Multiplier.**

 Abstract: This multiplier is based on the Gilbert Gain Cell, using two Gilbert Gain cells this multiplier was build. This Design is based on BJTs. **Tool used: Tanner** **Team Size: 2**

1. Title: **Mixers at GHz Frequencies**.

 Abstract: Two types of Mixers, one is Basic Mixer and the other is Mixer designed using Gilbert gain cell are studied. **Tool used: Tanner** **Team Size: 2**

1. Title: **Serial Link BUS: A low power On-Chip BUS architecture**.

 Abstract: In this architecture, Instead of n-bit conventional parallel-line bus we use n/m bus so that each m bits are serially send through 1 line. **Tool used: H-Spice**  **Team Size: 2**

1. Title: **Implementation of Low Density Parity Check Decoder.**

 Abstract: The decoder is implemented using verilog. It was simulated and synthesised in **FPGA advantage**. **Team Size: 2**

**B.E. Project**

1. Title: **Study of wavelets and their Applications.** (In Research center of Imarat (RCI), Hyderabad)

 Abstract: Studied the difference between wavelet transform and other transforms and various types of wavelets and there applications in different signal processing areas and finally I have removed the noise of a signal which is received from a target and compressed the size of an image by removing the high frequency contents of the image. **Team Size: 2**

**B.E. Mini Project**

1. Title: **Electronic Stethoscope**.

 Abstract: This circuit uses op-amps to greatly amplify a standard stethoscope, and includes a low pass filter to remove background noise. This Circuit is Designed on a general PCB board which consists of TL072 Low Noise Dual Op-Amp, 741 Op-Amp and LM386 Audio Power Amp as major parts and was powered by a 12-0-12 step down transformer and two regulators 7809 and 7909 to get the +9 and -9 volts Respectively. **Team Size: 1**

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| **Personal Strengths** |

* Hard working and good at team work.
* Rapid at learning things.

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| **Reference** |

Dr. M.B. Srinivas

Associate Professor
Chair, Centre for VLSI and Embedded System Technologies,

Head, Industry outreach Division
Chief Co-ordinator, Entrepreneurship Development Cell

IIIT-Hyderabad

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Dr. Satyam Mandavilli

Professor

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